contacts and the microprocessor. In rejecting this claim, the Office Action refers to the UART 7a of the Yamaguchi patent as corresponding to the claimed communication device. It is respectfully submitted, however, that the Yamaguchi patent does not disclose that the UART 7a comprises a hard-wired circuit disposed between the I/O terminal P5 and a microprocessor.

The Yamaguchi patent describes the background state of the prior art in connection with Figures 7 and 8. Figure 8 illustrates that the principal parts of an IC card comprise a microcomputer 20 and an EEPROM 30. As stated at column 2, lines 8-11, the microcomputer "includes functions corresponding to the CPU 1, the ROM 4, the RAM 6 and the input/output circuit 7 in Fig. 7." Thus, in the circuit configuration of Figure 8, the functionality of the input/output circuit is incorporated within the microcomputer.

Turning now to Figure 1, which illustrates the UART 7a, the patent states, at column 4, lines 20-24:

> An 1C card 100a shown in Fig. 1 is of the same basic configuration as the conventional IC card with standby function shown in Fig. 8, but Fig. 1 illustrates the IC card 100a in the form of functionally separated blocks.

Thus, the patent does not disclose that the UART 7a is a hard-wired circuit disposed between a microprocessor and contacts. Rather, consistent with the description of Figure 8, the UART 7a is incorporated within the microprocessor, rather than being a circuit that is separate therefrom. To the extent that it is represented by an individual block in Figure 1, that representation merely indicates one of the distinct functions performed by the microcomputer.

As such, therefore, the Yamaguchi patent is representative of the prior art that is described in the background section of the present application, in which the function of the input/output circuit is implemented within the microprocessor itself. Such a configuration requires some of the processing resources of the microprocessor, as well as some of its memory capacity, to be allocated to the I/O function. In contrast, the hard-wired circuit of the present invention relieves the microprocessor of this burden. For at least the foregoing reason, therefore, it is respectfully submitted that claims 1 and 6-8 are not anticipated by the Yamaguchi patent.

In addition to this distinction, claim 8 recites that the information generated by the generating means comprises an indication whether a command contained in a signal received from the terminal is complete and correct. The Office Action does not identify the basis for rejecting this claim. Applicants are unable to identify any teaching in the Yamaguchi patent that the UART 7a analyzes commands. It does not disclose that the UART attempts to determine whether a received byte pertains to a command, and if so whether that command is complete and correct.

For this additional reason, therefore, it is respectfully submitted that the subject matter of claim 8 is not anticipated by the Yamaguchi patent. If the rejection is not withdrawn, the Examiner is requested to identify the disclosure in the Yamaguchi patent that is being relied upon to support the rejection of claim 8.

Reconsideration and withdrawal of the rejection of claims 1 and 6-8, and allowance of all pending claims are respectfully requested.

Respectfully submitted,

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